

(54) SEMICONDUCTOR DISPLACEMENT TRANSDUCER

(11) 55-9406 (A)

(43) 23.1.1980 (19) JP

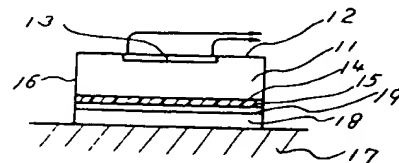
(21) Appl. No. 53-80991 (22) 5.7.1978

(71) HITACHI SEISAKUSHO K.K. (72) YASUTOSHI KURIHARA(1)

(51) Int. Cl.<sup>3</sup> H01L29/84//H01L21/58

**PURPOSE:** To increase accuracy of a transducer by restricting the density ratio of Ge not more than 12wt % to Au in an alloy solder that is used to combine a strain detecting body with a strain transferring element, thus maintaining uniform soldering.

**CONSTITUTION:** A semiconductor strain detecting body 16 has a strain sensing area 13 in the first main surface 12 of a single semiconductor crystal 11 and an insulating layer 15 on the second main surface 14 which is located in the same way as the surface 12. A strain transferring element 17 is made of an elastic metal. A solder layer 18 is made of an alloy. The semiconductor strain detecting body 16 and the strain transfer element 17 are integrated with a laminated body of the solder layer 18 and an intermediate metal layer 19 to constitute a displacement transducer. An Au - Ge alloy is used in the alloy solder layer 18 to enable soldering at low temperature and the range of the density ratio of Ge to Au in the solder is set to be not more than 12wt % in order to maintain uniform soldering. As a result, a uniform solder layer, without allowing precipitation of particles which have highly concentrated Ge, is obtained.



(54) SAMPLING TABLE FOR SCANNING ELECTRON MICROSCOPE ETC

(11) 55-9407 (A)

(43) 23.1.1980 (19) JP

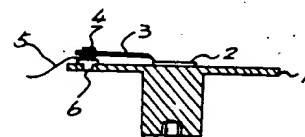
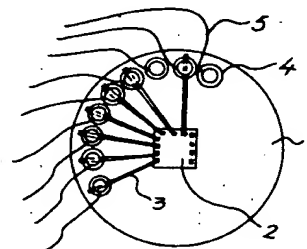
(21) Appl. No. 53-81013 (22) 5.7.1978

(71) HITACHI SEISAKUSHO K.K. (72) TADASHI OOTAKA(1)

(51) Int. Cl.<sup>3</sup> H01L21/66, H01J37/20

**PURPOSE:** To observe a surface potential image of an unbonded IC by providing several holders which are electrically insulated from a sampling table, and installing contacting probes to the holders on the sampling table, then applying voltage to the probes.

**CONSTITUTION:** A wafer consisting of an IC 2 is placed on the center of a sampling table 1, and through insulators 6, several holders 4 with contacting probes 3 attached to them are fixed on the periphery of the sampling table 1. The edges of these probes 3 are brought into contact with the edge of the IC 2, and voltage is applied through lead wires 5 which are connected to the holders 4. When the IC 2 is two-dimensionally scanned by means of an electron beam, signals being emitted from the IC 2 are shown on a CRT. By so doing, a surface potential image can be observed during manufacturing process before bonding the IC, thus enabling the analysis on the products and selection of good products. Therefore, manufacturing efficiency of the IC can be increased.



(54) REACTOR

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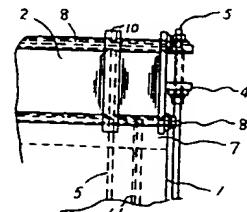
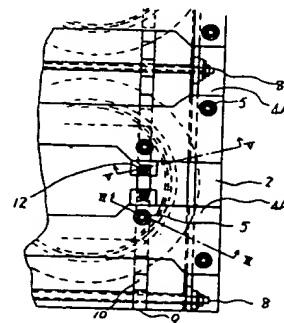
(21) Appl. No. 53-81018 (22) 5.7.1978

(71) HITACHI SEISAKUSHO K.K. (72) TAKASHI HAGITANI(2)

(51) Int. Cl.<sup>3</sup> H01F27/28, H01F27/30, H01F37/00

**PURPOSE:** To eliminate time required for drilling, as well as to reduce core loss by installing an insulation material inside an insulation sleeve to prevent a silicon steel plate from dislocation, thus eliminating through holes in a magnetic shield of the silicon steel plate.

**CONSTITUTION:** An insulator 7 which prevents a magnetic shield 2 of a silicon steel plate from dislocation, is installed in an insulation sleeve where a coil 1 of the magnetic shield 2 comes into contact. The insulator 7 is fixed to an upper metallic clamping tool 4A through a locking bolt 12 that is inserted into a gap 9 provided in the magnetic shield 2. As a result, the magnetic shield 2 is bound between the insulator 7 and the metallic clamping tool 4A. Securing the magnetic shield, in the silicon steel piling direction, is provided by the clamping tool 4 together with horizontal locking bolts 8 at above and below the magnetic shield 2. Consequently, time required for drilling the silicon steel plate is eliminated, and core loss is reduced.



# PATENT ABSTRACTS OF JAPAN

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(21)Application number : 53-081013

(71)Applicant :

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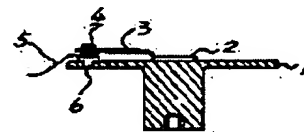
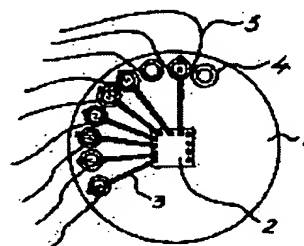
OTAKA TADASHI

KANDA KIMIO

**(54) SAMPLING TABLE FOR SCANNING ELECTRON MICROSCOPE ETC****(57) Abstract:**

**PURPOSE:** To observe a surface potential image of an unbonded IC by providing several holders which are electrically insulated from a sampling table, and installing contacting probes to the holders on the sampling table, then applying voltage to the probes.

**CONSTITUTION:** A wafer consisting of an IC 2 is placed on the center of a sampling table 1, and through insulators 6, several holders 4 with contacting probes 3 attached to them are fixed on the periphery of the sampling table 1. The edges of these probes 3 are brought into contact with the edge of the IC 2, and voltage is applied through lead wires 5 which are connected to the holders 4. When the IC 2 is two-dimensionally scanned by means of an electron beam, signals being emitted from the IC 2 are shown on a CRT. By so doing, a surface potential image can be observed during manufacturing process before bonding the IC, thus enabling the analysis on the products and selection of good products. Therefore, manufacturing efficiency of the IC can be increased.

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文庫3

⑨ 日本国特許庁 (JP)

⑩ 特許出願公開

⑫ 公開特許公報 (A)

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審査請求 有

(全 3 頁)

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⑱ 出 願 昭53(1978)7月5日

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明 細 書

発明の名称 走査形電子顕微鏡等の試料台

特許請求の範囲

1. 試料台の上に設けた試料の表面を電子ビームで2次的に走査し、上記試料が発生する信号によつて上記試料の表面像を得る走査形電子顕微鏡等において、上記試料台上に上記試料台とは電気的に絶縁された複数の保持具を設け、この保持具に上記試料に接触する接触針を取付けると共に、この接触針に電圧を印加するとく形成したことを特徴とする走査形電子顕微鏡等の試料台。

2. 試料台の上に設けた試料の表面を電子ビームで2次的に走査し、上記試料が発生する信号によつて上記試料の表面像を得る走査形電子顕微鏡等において、上記試料台の周辺部に複数の小孔を設け、この小孔に回転可能に嵌入装着させた軸を有する絶縁体と、この絶縁体上に固定し上記試料台の表面と平行な方向のねじ穴およびこのねじ穴の底部に小径の貫通孔を設けた金

属製のガイドホルダーと、このガイドホルダーの上記貫通孔を貫通すると共に上記ねじ穴に収容された圧縮ばねおよび上記ねじ穴に嵌合させたねじによつて移動可能に支持された接触針とで形成した保持具を複数個設け、上記ガイドホルダーに通電し上記接触針を介して上記試料に電圧を印加することを特徴とする走査形電子顕微鏡等の試料台。

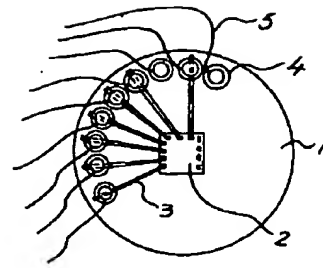
3. 上記試料が、上記試料台上に微動可能に設置されたウエハ上の集積回路である特許請求の範囲第2項記載の走査形電子顕微鏡等の試料台。

発明の詳細な説明

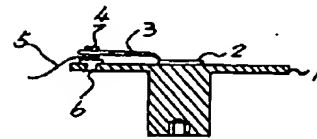
本発明は走査形電子顕微鏡等の試料台に係り、特に、集積回路の表面状態を観察するための試料台に関するものである。

従来、集積回路の動作試験時の状態を走査形電子顕微鏡等(以後SEMと記す)で観察するには、集積回路の端子に電圧を印加して表面電位像をCRT上に表示していた。特に、最近是集積回路が大型複雑化したので、この表面電位像による検

第1図



第2図



検査することができる。第3には、SEMが備えている試料微動装置を有効に利用することができるので、保持具は比較的簡単安価に構成することができしかも多機能である。

なお、第1図、第2図では1箇の集積回路を検査する場合を図示してあるが、複数の集積回路を1枚のウェハ上に構成した切断前の集積回路についても同様に検査することができる。

以上本発明のSEMの試料台は、製造工程中の集積回路を能率的に検査することができるという効果をもっている。

図面の簡単な説明

第1図は本発明の一実施例である試料台の平面図、第2図は第1図の試料台の垂直断面図、第3図は第2図の保持具の拡大断面図である。

1…試料台、2…集積回路、3…接触針、4…保持具、5…リード線、6…絶縁体、7…ガイドホルダー、8…圧縮ばね、9…ねじ。

代理人 弁理士 高橋明夫

第3図

